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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ta-Chin Lin, Yi-Feng Huang, Fu-Kang Lai and Jen-Chih Hsiao  
Application Serial No.: 10/672,403

Filed: September 26, 2003

For: Algorithms Tunning for Dynamic Lot Dispatching in Wafer and Chip Probing

Patent No.: Unassigned

Issue Date: Unassigned

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia 22313-1450

### **CERTIFICATE UNDER 37 C.F.R. §3.73(b) ESTABLISHING RIGHT OF ASSIGNEE TO TAKE ACTION**

1. The assignee of the entire right, title and interest hereby seeks to take action in the PTO in this matter.

#### **IDENTIFICATION OF ASSIGNEE**

2. The assignee of this matter is:

#### **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**

8, Li-Hsin Rd. 6  
Hsinchu Science Park  
Hsinchu, Taiwan 300-77, R.O.C.

#### **PERSON AUTHORIZED TO SIGN**

3. Daniel R. McClure  
Attorney for Assignee

4. A chain of title from the inventor(s) to the current assignee is shown below:

a. From: Ta-Chin Lin, Yi-Feng Huang, Fu-Kang Lai and Jen-Chih Hsiao  
To: Taiwan Semiconductor Manufacturing Company, Ltd.  
Recorded in PTO: Reel: 014554 Frame: 0202

**DECLARATIONS**

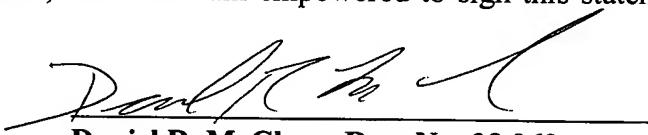
5. I, the undersigned, have reviewed all the documents in the chain of title of the

application  
 patent

matter identified above and, to the best of my knowledge and belief, title is in the assignee identified above.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

7. I, the person signing below, aver that I am empowered to sign this statement on behalf of the assignee.



Daniel R. McClure, Reg. No. 38,962

Tel. No. 770-933-9500

Customer No.: 24504

Docket No. 252016-2460

**THOMAS, KAYDEN, HORSTEMEYER  
& RISLEY, L.L.P.**  
100 Galleria Parkway, Suite 1750  
Atlanta, Georgia 30339-5948



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:

Application No.:

Filed:

Title:

Commissioner for Patents

Washington, D.C. 20231

**POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST**  
**(REVOCATION OF PRIOR POWERS)**

As assignee of record of each of the patent applications listed in the table of attachment A,

**REVOCATION OF PRIOR POWERS OF ATTORNEY**

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

**NEW POWER OF ATTORNEY**

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

**000047390**

Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962  
**THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.**  
100 Galleria Parkway, Suite 1750  
Atlanta, Georgia 30339  
770-933-9500

**ASSIGNEE OF ENTIRE INTEREST**

**TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**  
8, Li-Hsin Rd. 6  
Hsinchu Science Park  
Hsinchu, Taiwan 300-77, R.O.C.

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ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: Nov. 25, 2004

*Chien-Wei Chou*

Chien-Wei (Chris) Chou  
Director - Intellectual Property Division

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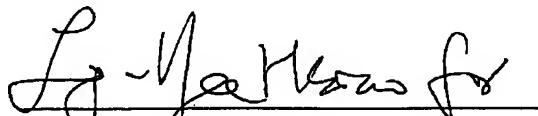
## Attachment A

| No. | Serial No  | TSMC No    | Application Title   | Filing Date | Assignment (Reel/Frame)  |
|-----|------------|------------|---|-------------|--|
| 1   | 10/140,647 | 2001-0941  | Prober Index Control for Remote Debugging by Web Browser                                      | 5/7/02      | 012902/0473  |
| 2   | 10/725,810 | 2001-0972  | Method of the Adjustable Matching Map System in Lithography                                   | 12/2/03     | 014761/0759  |
| 3   | 10/694,426 | 2001-1094  | Method of a Floating Pattern Loading System in Mask Dry-Etching Critical Dimension Control    | 10/27/03    | 015067/0473  |
| 4   | 10/672,403 | 2001-1457  | Algorithms Tuning for Dynamic Lot Dispatching in Wafer and Chip Probing                       | 9/26/03     | 014554/0202  |
| 5   | 10/286,626 | 2001-1265  | Application of Impressed-Current Cathodic Protection to Prevent Metal Corrosion and Oxidation | 11/2/02     | 013469/0539  |
| 6   | 10/134,820 | 2001-1349  | Method for Measuring Gate-To-Body Current of Floating-Body PD SOI MOS Devices                 | 4/26/02     | 012869/0369  |
| 7   | 10/822,197 | 2001-1440C | Embedded DRAM for Metal-Insulator-Metal (MIM) Capacitor Structure                             | 4/9/04      | Recorded<br>013982/0163<br>at the parent application<br>USP6,720,232 |
| 8   | 10/749,698 | 2001-1510  | Multivariate RBR Tool Aging Adjuster  | 12/31/03    | 014877/0720  |
| 9   | 10/081,985 | 2001-0725  | Adjustment of N and K Values in a Darc Film   | 2/21/02     | 012644/0807  |
| 10  | 10/788,173 | 2001-1543  | Chip Probing Equipment and Test Modeling for Next Generation MES(300MM)                       | 2/26/04     | 015033/0283  |
| 11  | 10/631,842 | 2002-0228  | Method to Form Self-Aligned Floating Gate to Diffusion Structures in Flash                    | 7/31/03     | Filed 7/31/03  |
| 12  | 10/406,122 | 2001-0938  | High Performance Color Filter Process for Image Sensor  | 4/3/03      | 014181/0899  |
| 13  | 10/420,594 | 2001-0452B | Method to Fabricate Self-Aligned Source and Drain in Split Gate Flash                         | 4/22/03     | Recorded<br>012656/0769<br>at the parent application<br>USP6,573,142 |
| 14  | 10/189,874 | 2001-0427  | SCR-ESD Structures with Shallow Trench Isolation  | 7/5/02      | 013086/0425  |
| 15  | 10/726,105 | 2001-0427B | SCR-ESD Structures with Shallow Trench Isolation  | 12/2/03     | Recorded<br>013086/0425<br>at the parent application<br>USP6,720,622 |

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|    |            |            |   |          |  |
|----|------------|------------|---|----------|--|
| 16 | 10/810,965 | 2001-0413C | Novel Method to Improve Bump Reliability for Flip Chip Device               | 3/26/04  | Recorded 012573/0276 at the parent application USP6,756,294  |
| 17 | 10/058,474 | 2001-0353  | Electronic Customs Release Slip (E-CRS)                                     | 1/28/02  | 012553/0539  |
| 18 | 10/725,852 | 2001-0088B | Effective Vcc to Vss Power ESD Protection Device                            | 12/2/03  | Recorded 014859/0845 at the parent application USP6,682,993  |
| 19 | 10/357,136 | 2001-0043B | Novel Low Leakage Current Cascaded Diode Structure                          | 2/3/03   | Recorded 012326/0168 at the parent application USP6,537,868  |
| 20 | 10/626,778 | 2000-0659B | Novel Test Structure for Detecting Bridging of DRAM Capacitors              | 7/24/03  | Recorded 011732/0773 at the parent application USP6,617,180  |
| 21 | 10/186,579 | 2000-0307B | Lossless Co-Planar Wave Guide in CMOS Process                               | 7/1/02   | Recorded 011498/0374 at the parent application USP6,465, 367 |
| 22 | 10/272,086 | 2002-0227  | Method to Form Self-Aligned Split Gate Flash with L-Shaped Wordline Spacers | 10/16/02 | 013408/0312  |

Date: Nov. 25, 2004

  
 Chien-Wei (Chris) Chou  
 Director - Intellectual Property Division

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